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HIGH CONTRAST ELECTROLUMINESCENT NUMERIC READOUT DEVICE.(U)
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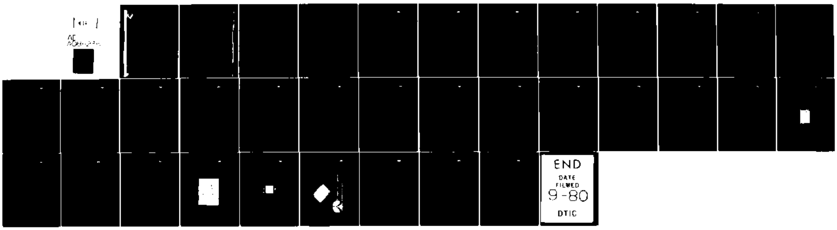
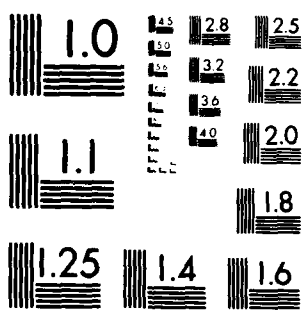
UNCLASSIFIED ERC41016.15IRF DELET-TR-78-2996-2 NL





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Research and Development Technical Report

DELET-TR-78-2996-2

HIGH CONTRAST ELECTROLUMINESCENT NUMERIC READOUT DEVICE

M. K. Kilcoyne
ROCKWELL INTERNATIONAL
Thousand Oaks, CA 91360

August 1980

Second Interim Report for Period 1 Feb. 79 – 31 May 79

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1. REPORT NUMBER: DELET-TR-78-2996-2 — 2. GOVT ACCESSION NO.: AD-A088 238	3. RECIPIENT'S CATALOG NUMBER
4. TITLE (and Subtitle): HIGH CONTRAST ELECTROLUMINESCENT READOUT DEVICE	5. TYPE OF REPORT & PERIOD COVERED: Interim Technical Report. 1 Feb [redacted]79 [redacted]-31 May [redacted]79
	6. PERFORMING ORG. REPORT NUMBER: ERC41016.15IRF
7. AUTHOR(s): M. K. Kilcoyne	8. CONTRACT OR GRANT NUMBER(s): DAAB07-78-C-2996
9. PERFORMING ORGANIZATION NAME AND ADDRESS: Electronics Research Center, Rockwell International Corporation, Thousand Oaks, CA 91360	10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS: 62705A ILI62705AH94 03 DIIC8
11. CONTROLLING OFFICE NAME AND ADDRESS: Electronic Technology & Devices Laboratory, ATTN: DELET-BD, Ft. Monmouth, NJ 07703	12. REPORT DATE: Aug [redacted] 80
	13. NUMBER OF PAGES: 30
14. MONITORING AGENCY NAME & ADDRESS (if different from Controlling Office)	15. SECURITY CLASS. (of this report): Unclassified
	15a. DECLASSIFICATION/DOWNGRADING SCHEDULE

16. DISTRIBUTION STATEMENT (of this Report)

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17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)

18. SUPPLEMENTARY NOTES

19. KEY WORDS (Continue on reverse side if necessary and identify by block number)

Thin film
High-contrast
Numeric Display

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

The Rockwell International Electronics Research Center has completed the second phase of the development program encompassing the design, fabrication, and characterization of experimental models of a high-contrast numeric electroluminescent readout device. This device consists of two-digits of seven-segment numeric displays using a transparent electroluminescent thin film with high-contrast background layer. The device also contains within its hermetically sealed package, logic and drive circuitry to operate the numeric displays from a typical computer output data processing information, with five volt T²L logic

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level and BCD input.

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1. SUMMARY

The Rockwell Electronics Research Center has completed the second phase of the development program encompassing the design, fabrication, and characterization of experimental models of a high-contrast numeric electroluminescent readout device. This device consists of two-digits of seven-segment numeric displays using a transparent electroluminescent thin film with high-contrast background layer. The device also contains with its hermetically sealed package, logic and drive circuitry to operate the numeric displays from a typical computer output data processing information, with five volt T^2L logic level and BCD input. The package design also allows the devices to be arranged so that a multi-digit computer-type terminal readout can be fabricated from a series of individual packages.

This report covers the work completed during the fourth through the eighth months of effort. During this period, logic and decoder electronics have been committed to a semi-custom integrated circuit chip design. Several designs for high-voltage drivers were evaluated and the final high-voltage driver approach selected. A process has been developed for hermetic sealed packages having vertical interconnects for transmitting signals from the driver electronics vertically to the thin film EL display. Further electrical and optical tests have been conducted on high-contrast materials and on sample EL devices to characterize electro-optical parameters. Evaluation and analysis of these results are reviewed in detail in the following sections.

2. PROGRAM AIMS AND OBJECTIVES

The objective of this program is to design and fabricate a quantity of numeric EL display devices containing two-digits consisting of seven segments and a decimal point. Four (4) exploratory development models will be fabricated each consisting of a ten-digit display made up of five of the two-digit numeric devices assembled into a suitable socket or printed circuitboard. Drive circuitry and decoding logic will be included in the device to allow operation directly from computer level logic inputs at TTL voltage levels. The display medium shall be a transparent AC thin film electroluminescent type with a high-contrast background layer for viewing in high-light ambience. The operational characteristics of the devices shall be designed to allow uniform electronic dimming of the display to luminance levels in the order of the 10^{-3} ft-L for compatability with night vision applications. The display shall be capable of sufficient contrast to be viewed in an ambient illumination of 10,000 ft-C without additional contrast enhancement techniques. The devices shall be capable of operation for a minimum of 3,000 hours at a luminance level that satisfies the condition of visibility under high-ambient illumination described above. Also, the devices shall operate without the loss of significant light emitting areas due to any failure or degradation mechanism during the 3,000 hour/lifetime.

3. DECODER - DRIVER CIRCUIT DESIGN AND FABRICATION

3.1 Logic Circuit Design

Figure 1 shows the original circuit in which the logic functions and driver circuitry were evaluated. Figure 2 shows the circuit resulting from that evaluation from which the design for the semi-custom integrated logic chip was taken. To accommodate multi-digit displays one modification was made from the original circuit. The digit select and enable functions on pin five and pin six, (Fig. 1), were modified to a digit strobe circuit in which either digit can be selected with its own strobe pulse. This modification was made as a simplification for addressing multiple chips of two digits each so that all digits are directly accessible by means of a strobe without the necessity of a digit select function.

The functions on the logic chip consist basically as follows:

A five KHz clock is used to generate the drive frequency for the AC operation of the TFEL display. The circuit utilizes a latched BCD to 7-segment decoder/driver signal circuit. The 7-segment output signals are toggled by the display frequency input which causes the selected segment outputs to be a square wave at the clock input frequency. With the clock frequency square wave present the selected segments will have a square wave output that is 180°C out of phase with the display frequency input. Those segments which are not selected will have a square wave output that is in phase with the input.

The mask layout and bonding pad designations have been received from the vendor. After some modifications to simplify hybrid circuit layout,

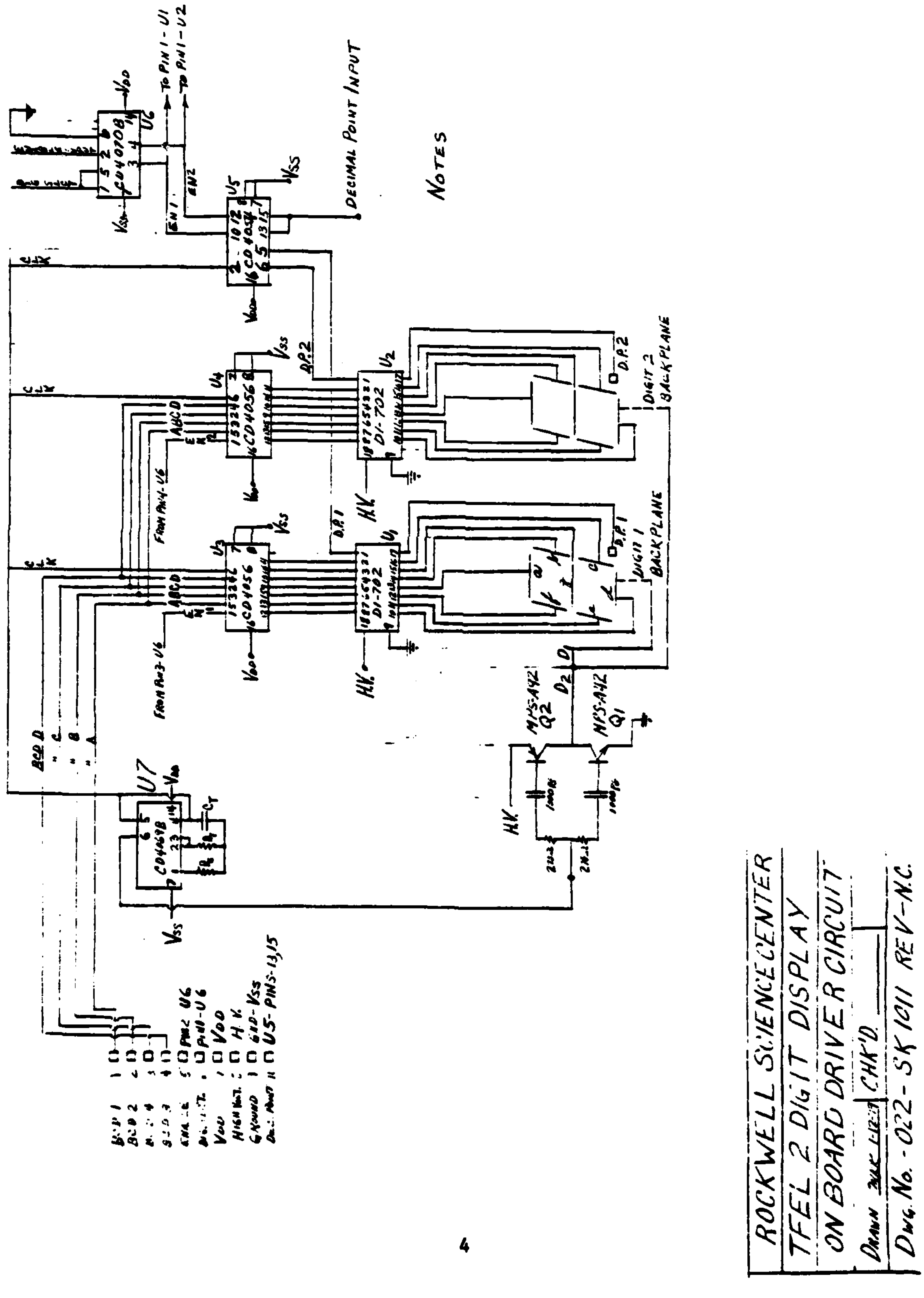

Fig. 1 Original Breadboard Circuit Schematic

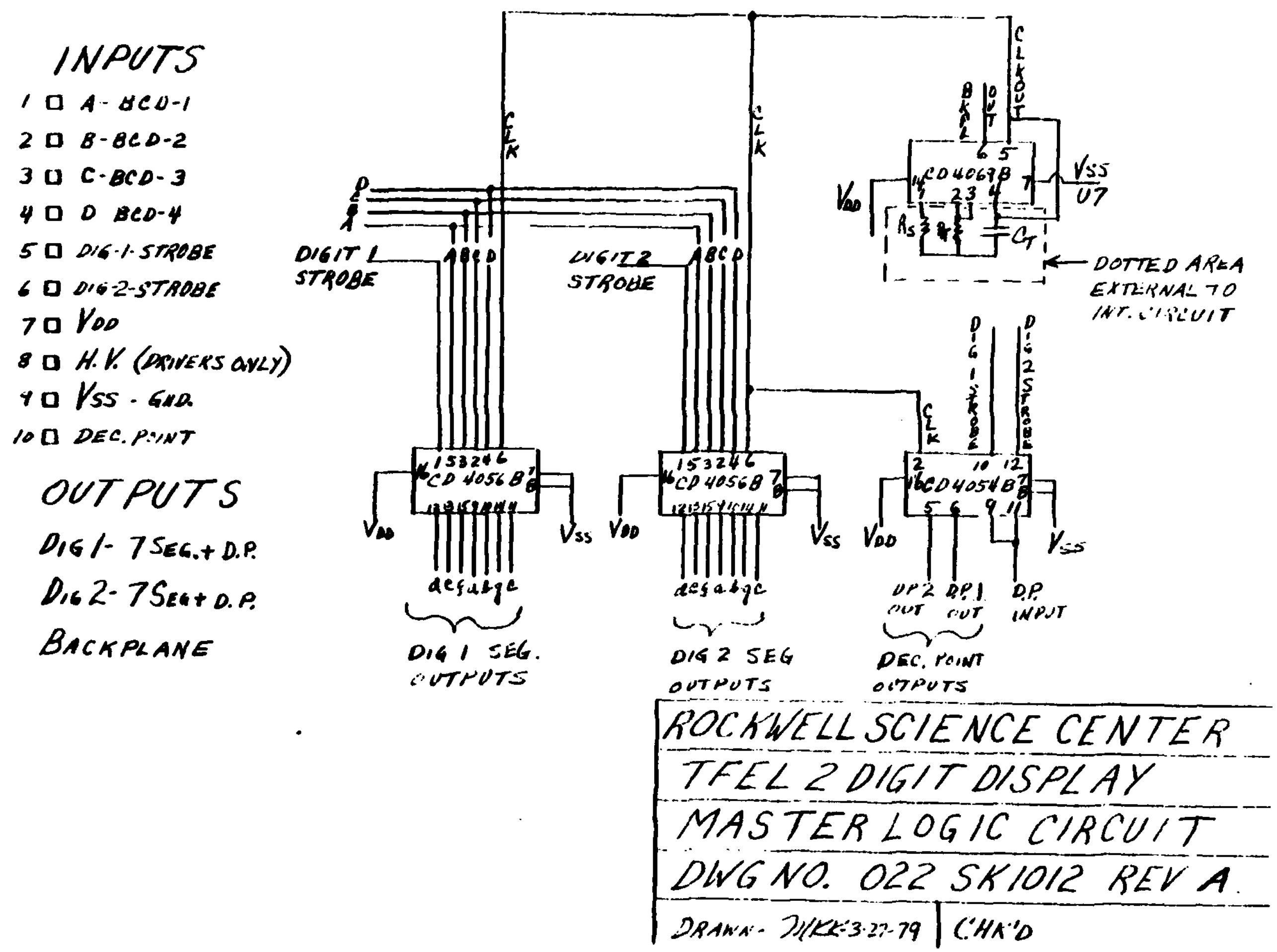

Fig. 2 Semicustom Logic Chip Schematic

the pinouts have been finalized as shown in Fig. 3. A complete listing of pinouts and bonding pad designations are given in Table I. In the table pin numbers refer to the pinouts in the 40-pin package in which the first samples will be received for design verification. The package chips will also be utilized for evaluation with the high-voltage test chips referred to in a later section of this report. The packaged logic chips will be evaluated with the high-voltage test chips driving EL numeric displays to assure total design compatibility.

The chip bonding pads are designated by letters and refer to the bonding locations on the die for hybrid circuit layout considerations in the two-digit package. The chip site (bonding pad) locations have been optimized for the hybrid circuit layout with respect to high-voltage driver chip input locations.

The five KHz oscillator circuit is driven from bonding pad locations RR, SS, and TT.

The chip consists of a logic circuit to decode incoming BCD information and also contains active components of the five KHz onboard oscillator circuit. The pas. ve components of the five KHz oscillator are shown in Fig. 3 in schematic form they are connected to pads RR, SS, and TT.

3.2 <u>High-Voltage Driver Circuit Design</u>

The original prototype circuit shown in Fig. 1 references a dionics DI 702 high-voltage driver array chip. However, test driver arrays provided by the vendor did not meet voltage and current requirements as originally proposed by the vendor. Further samples also failed to meet requirements and, therefore, a discrete transistor driver array was used in prototype evaluation.

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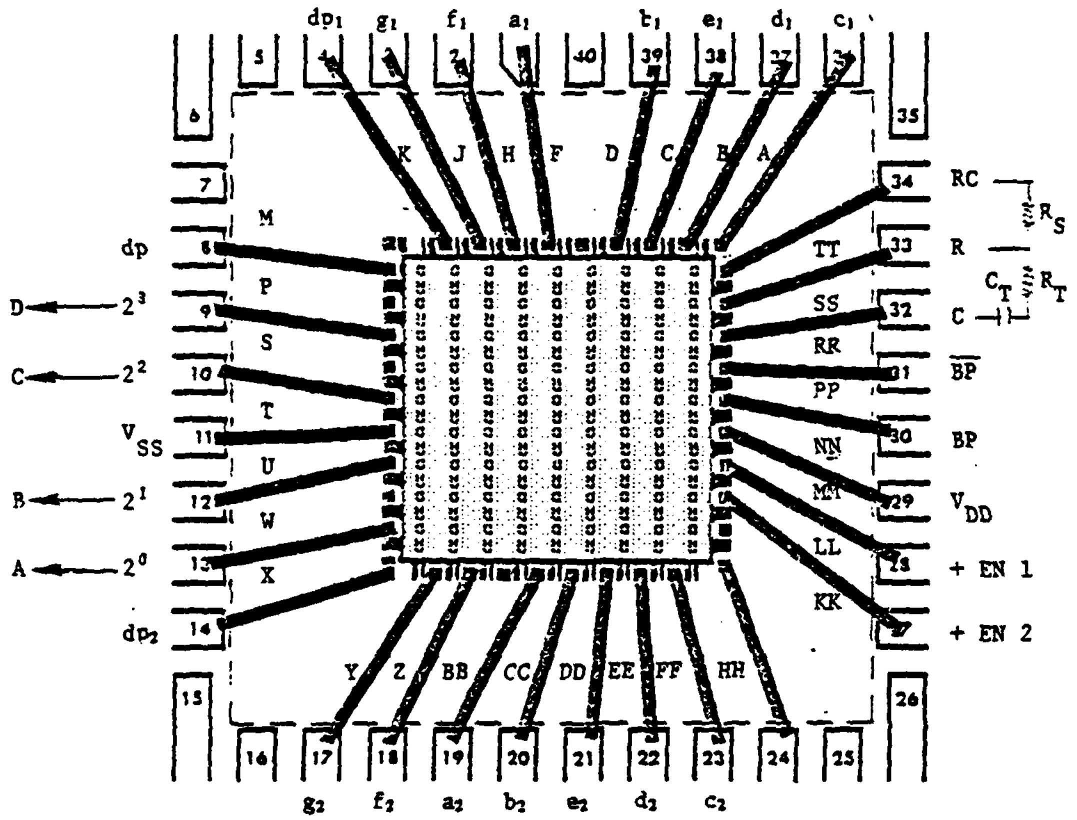
ASSEMBLY DIAGRAM 40-PIN DUAL-IN-LINE

ERC41016.15IRF



DATE: 29 August 1979 INITIALS: CAA/PCA

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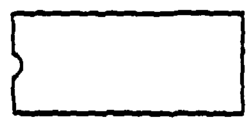


DIE NUMBER: RI 154

DIE SIZE: 136 x 136

SPECIAL INSTRUCTIONS: Special - Not for production

Fig. 3 Logic Chip Diagram with Pinouts

TABLE I

PINOUT (TENTATIVE)

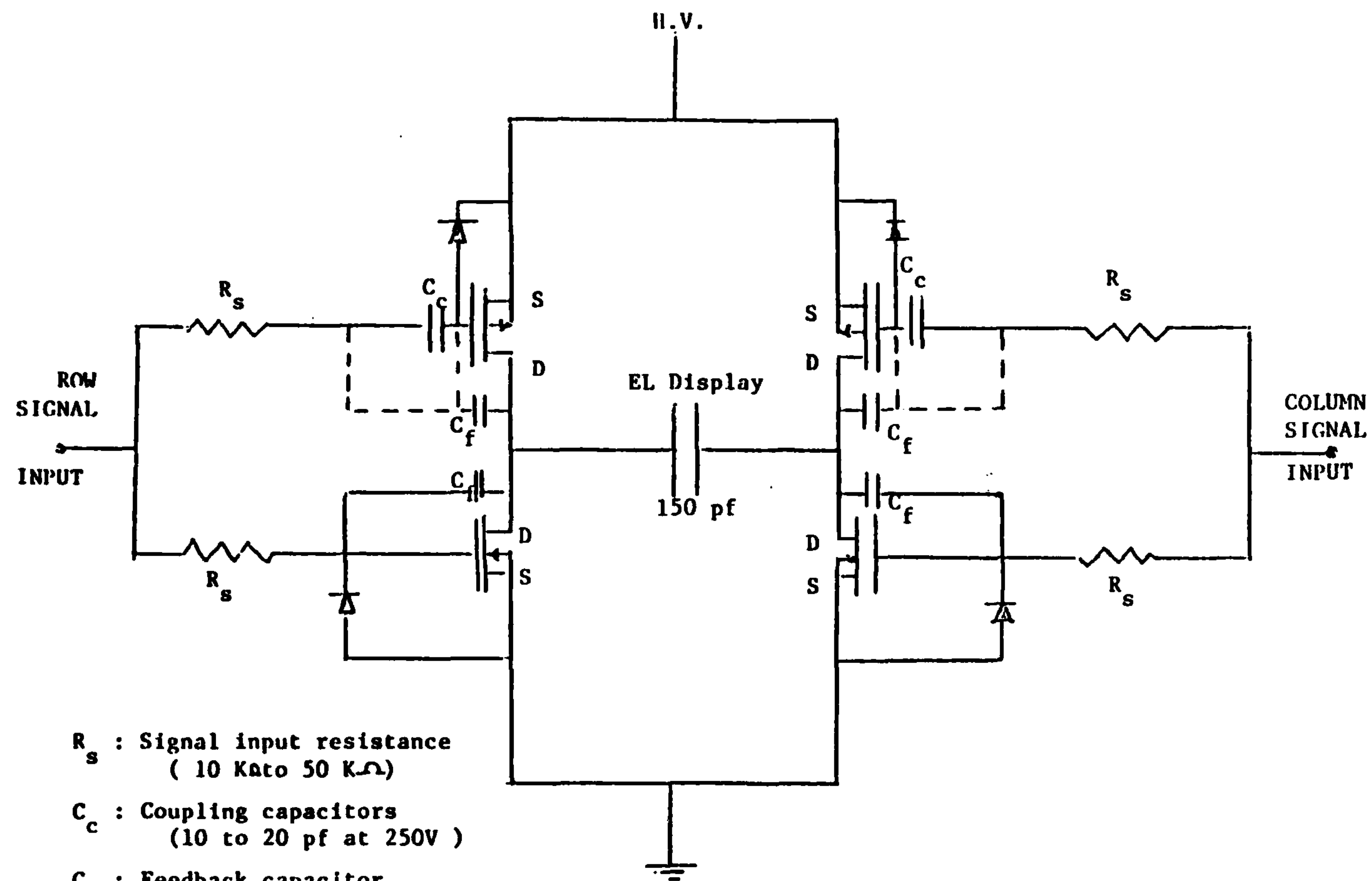
PIN #	CHIPSITE	CIRCUIT NAME
1	F	a_1
2	H	f_1
3	J	g_1
4	K	dp_1
5		
6		
7		
8	M	dp
9	P	2^3
10	S	2^2
11	T	V_{SS}
12	U	2^1
13	W	2^0
14	X	dp_2
15		
16		
17	Y	g_2
18	Z	f_2
19	BB	a_2
20	CC	b_2
21	DD	e_2
22	EE	d_2
23	FF	c_2
24	HH	
25		
26		
27	KK	+ Enable 2
28	LL	+ Enable 1
29	MM	V_{DD}
30	NN	BP
31	PP	$\overline{BP}$
32	RR	C
33	SS	R
34	TT	RC
35		
36	A	c_1
37	B	d_1
38	C	e_1
39	D	b_1
40		

The originally proposed chips would not meet requirements, several other approaches to the high-voltage drivers were evaluated. While several approaches would meet electrical requirements, these circuits were in discrete form and not available in integrated array chips necessary to meet size and space requirements in the two-digit EL display package.

Fortunately, Rockwell in a similar program, has under development a DMOS high-voltage driver array chip. Since this chip is not available until late December, 1979, a delay in the program would be required to utilize the DMOS driver chip. The timing was discussed with the contract monitor and a request for delay of final hardware deliveries has been proposed to allow utilization of the DMOS driver arrays.

Table II shows a time schedule of development of the devices. The program is divided into two phases. Phase one involves designing test masks and fabricating test devices in order to optimize device performance and device processing. The second phase will involve the integration of the optimized processing into a single chip containing nine n-channel and nine p-channel MOSFETS connected in complimentary pair arrays. Each array (see Fig. 4) will consist of an n- and a p-channel device with the necessary resistors and coupling capacitors required for signal switching and wave shaping.

There are several major advantages of the complimentary DMOS process over the bi-polar approach. First of course, is the direct interface compatibility to other CMOS logic circuitry. Secondly, the MOSFET devices have negligilbe leakage currents in the gates and therefore negligible



R_s : Signal input resistance
(10 Kato 50 KΩ)

C_c : Coupling capacitors
(10 to 20 pf at 250V)

C_f : Feedback capacitor
(Rise time about 5 to 10 μsec.)

EL : Electroluminescence Display
(150 pf/ driven element line)

Fig. 4 High-Voltage DMOS Driver Circuit

charged storage problems. This results in much smaller coupling capacitors required for voltage isolation from the logic circuitry. Turn off and turn on delay times of 10 to 20 nano seconds show the high speed response of the DMOSFET. Another advantage is more packing density per unit area with the MOS process than is possible with bi-polar devices due to their dielectric isolation requirements. Also, the more simplified DMOS process results in significantly lower cost. Based on quotations for both technologies, the volume cost of the DMOS integrated circuit chips was about one third of that for the bi-polar approach. In addition, the bi-polar approach was available only in separate chips one having npn and the other pnp devices.

The first phase of the DMOS transistor development should be completed by September, high-voltage transistor arrays will be available by December, 1979.

3.2.1 Test Chip Layout

Figure 5 shows the layout of the test chip. The chip will have in one section 40 test cells to allow for variation of the parameters to optimize the cell characteristics. Also, as seen on the chip other test components will be included for the purposes of evaluating chip processing and doping levels and also for stitch bonding "outboard" capacitors and resistors and other components such as small MOSFETS and invertors which may be used for various circuit purposes. The total chip size of the test chip is 100 x 155 mils. The test chip will be processed in both n-channel and p-channel versions and chips of this type will be available in September, 1979.

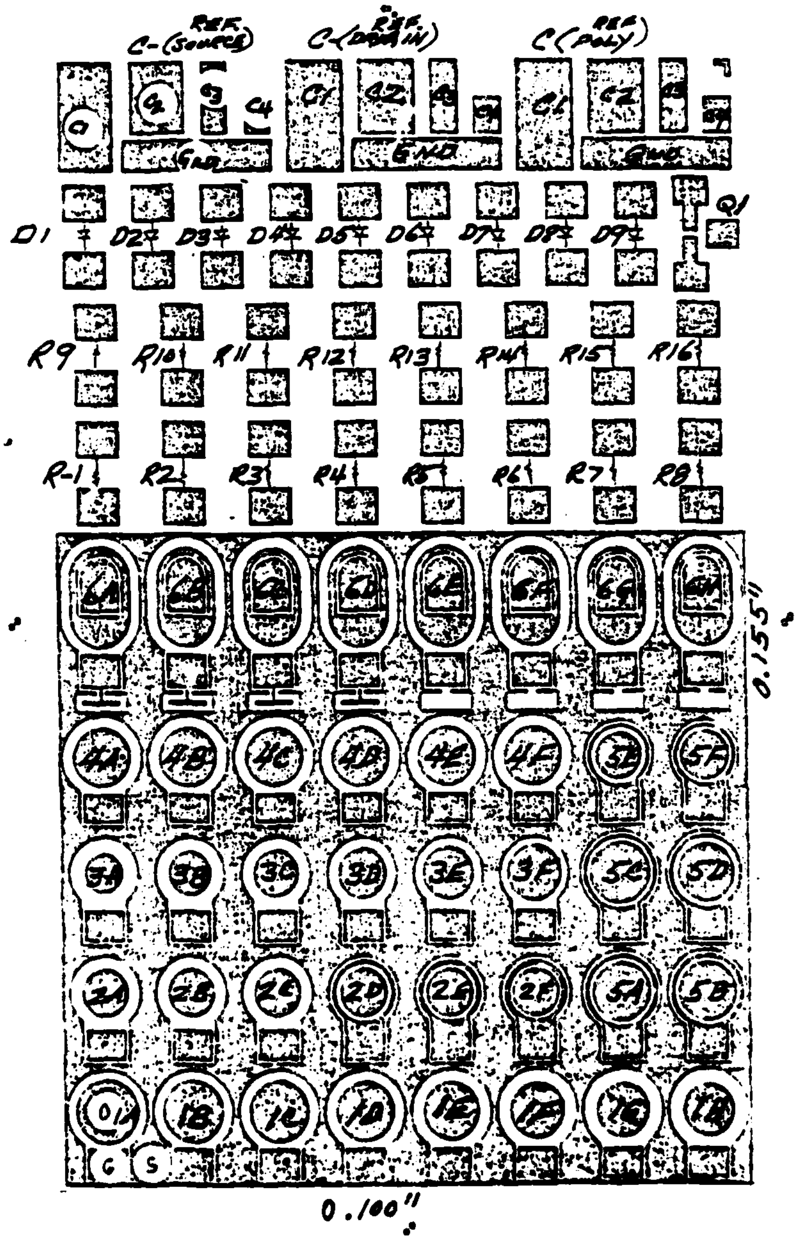


Fig. 5 High-Voltage Test Chip Layout

3.2.2 Complimentary High-Voltage Driver Array

The diagram depicting the complimentary DMOS approach is shown conceptually in Fig. 6. In this approach the n^- wafer would be used as anticipated for non-epi n-channel processing. The process steps would be essentially those for non-epi processing. In addtion, a large p-well would be difused into the surface creating a p^- lightly doped area which would withstand 250 volts from the substrate with acceptable leakage levels. This approach would allow the processing of an n-channel device within the p-well on the same chip with both n- and p-channel devices having 250 volts source to drain voltage switching capability.

Figure 7 shows the proposed high-voltage complimentary driver array. The device has already been size estimated by the vendor at 100 x 120 mils per complimentary chip containing nine p-channel and n-channel drivers as described above. The vendor has agreed to give the complimentary approach the highest priority as it substantially simplifies assembly and reduces assembly cost and complexity. The vendor already has demonstrated 400 volt switching capability on n-channel and p-channel devices and separate chips which can be utilized if necessary.

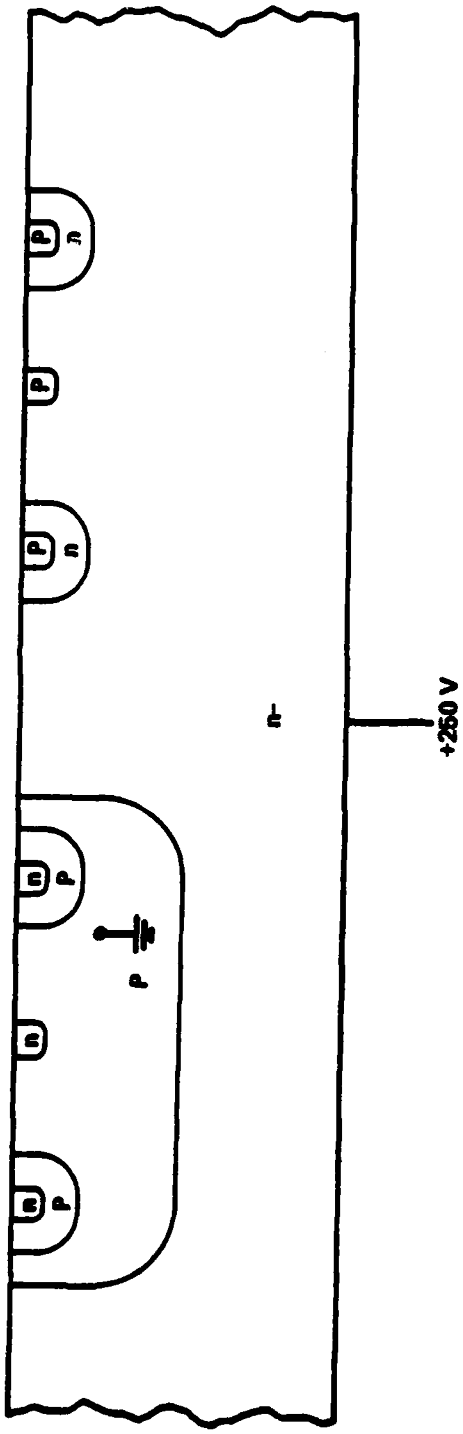


Fig. 6 Complimentary DMOS Approach

HIGH VOLTAGE DRIVER ARRAY

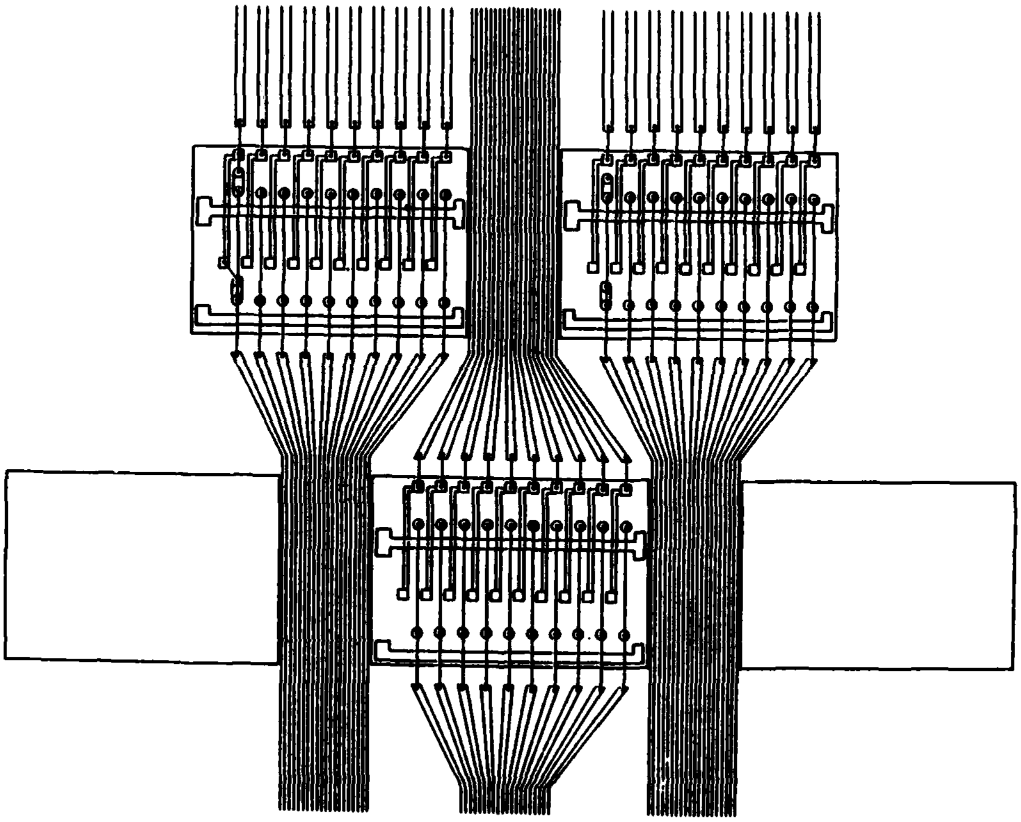


Figure 7

4. HYBRID CIRCUIT LAYOUT AND ASSEMBLY

Since the master logic chip has been defined and the high-voltage driver chip approximate size and layout have been estimated by the vendor, design evaluation of the hybrid circuit layout can be initiated. Table III shows the area requirements for the integrated circuit chips with allowances for die bonding and wire bonding. Additional area requirements for conductor path routing to display interconnects is also estimated to obtain an overall assessment of total hybrid circuit area requirements.

The hybrid circuit has six chips one of which is a logic chip to decode the incoming BCD information. The logic chip also contains active components of the five KHz oscillator circuit which requires two resistors and a capacitor not availble on the semi-custom CMOS logic chip. Two high-voltage driver chips are also required bringing the total to six chips. The high-voltage driver chips have nine complimentary pair drivers on each chip to accommodate seven segments, a decimal point, and a back-plane electrode.

The total area required of the hybrid circuit (Table III) is estimated at 205,386 square mils which is substantially greater than the area available for a single level circuit layout (120,610). A two or three level circuit will be required to accommodate conductor routings. In production quantities, a multi-layer ceramic with vertically conducting vias can be tooled to provide two or three layer circuitry as well as the vertical interconnects and seal area to the display. This method of laminating layers of unfired but screened ceramic tape to form a multi-layer composite is now routinely applied in specialized multi-layer hybrid circuitry.

TABLE II

High-Voltage Driver Development Schedule

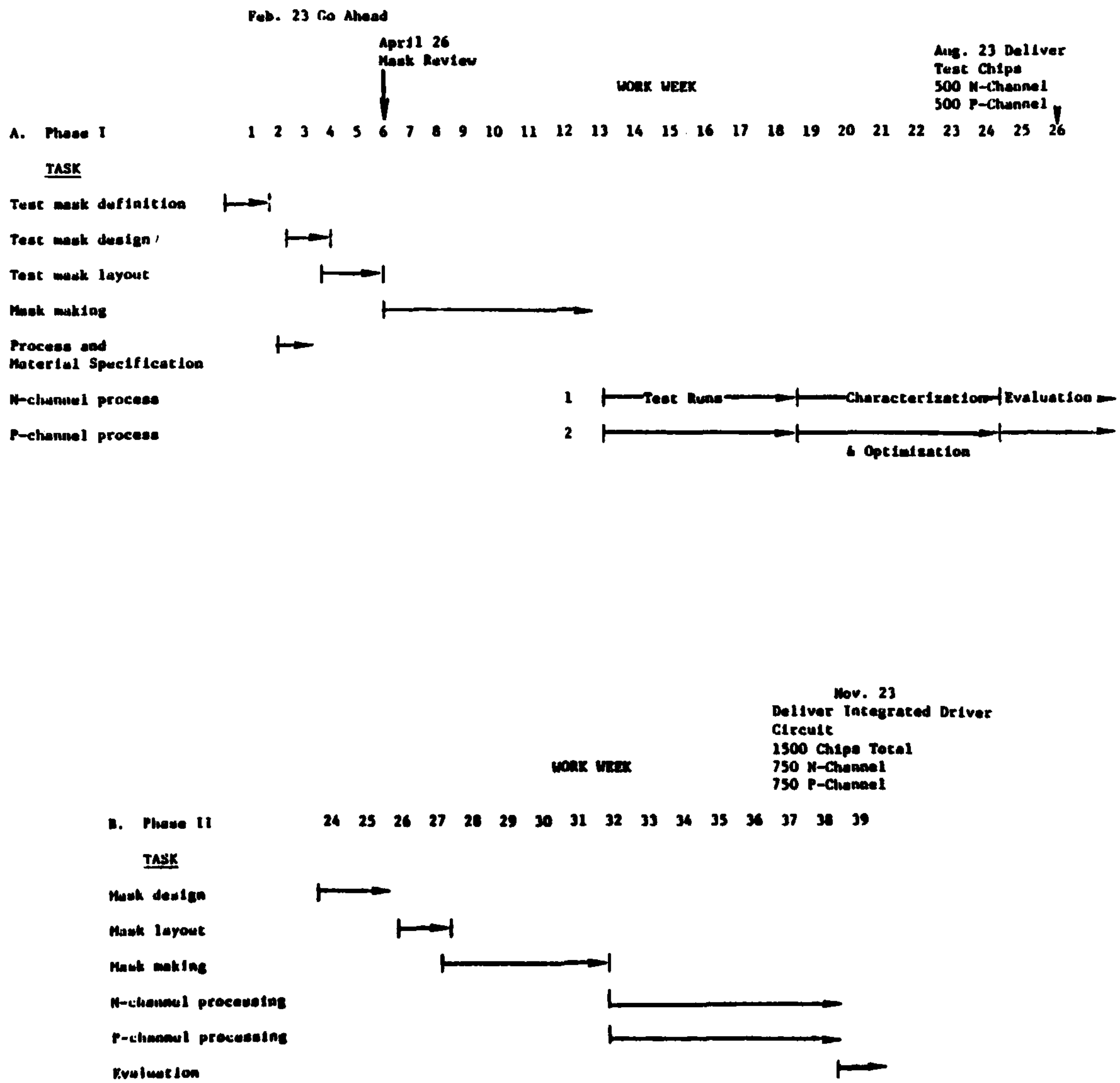


TABLE III

CHIP/FUNCTION	DIMENSION MILS	AREA SQ. MILS	AREA INCLUDING DIE BONDING-SQ. MILS	AREA INCLUDING WIRE BONDING ALLOWANCE-SQ. MILS
Logic Chip	136 x 136	18,496	21,316	30,976
Capacitor/Osc.	40 x 50	2,000	3,000	3,000
Resistor/Osc.	40 x 50	2,000	3,000	3,000
Resistor/Osc. Stability	40 x 50	2,000	3,000	3,000
High Voltage Driver Diagram 1	100 x 120	12,000	14,300	22,400
High Voltage Driver Diagram 2	100 x 120	12,000	14,300	22,400
SUB-TOTALS		48,496	58,916	84,776
Area required for conductor routing to display				120,610
Total area required - hybrid circuit				205,386*
Area available - hybrid circuit - 1 level				128,000
Area available - hybrid circuit - 2 levels				230,400
Area available - hybrid circuit - 3 levels				332,800

* Total hybrid circuit area required may be reduced somewhat in 2 & 3 level circuitry where crossovers and vias may reduce conductor path lengths.

5. HIGH-CONTRAST DISPLAY PERFORMANCE

A design for high-contrast EL displays utilizing conductive high-contrast layers has been implemented. The approach utilizes a light abosrbing insulator film in combination with a transparent conductive coating that closely matches the refractive index of the 7059 glass substrate material. Since both the light absorbing film and the transparent conductor closely match the index of the substrate front surface, reflections are substantially reduced as suggested by measurements reported in Interim Report # 1.

The light absorbing film is utilized in all areas of the display that are not active. Reflections in the active segment areas are reduced by controlling the total thickness of the phosphor insulator sandwich so that it is in an interference mode over the visible spectrum. In addition, a conductive light absorbing film is applied between the phosphor and the metal book electrode.

Figure 8 shows a cross sectional view of the display design, showing the location of the various layers. The active segment areas are defined by the openings in the light absorbing film. Devices with this structure have been fabricated and are presently being characterized. Test data will be reported in the next monthly progress letter.

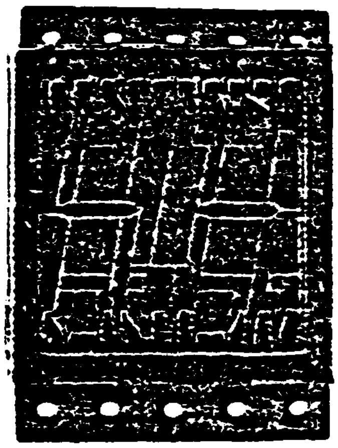


Fig. 8 High-Contrast Display Configuration

6. HERMETIC SEAL DESIGN AND FABRICATION

6.1 Requirements

The design for the hermetically sealed package for the high-contrast EL numeric display with on-board decoder-driver electronics must meet several requirements:

1. Hermeticity $<10^{-8}$ std cc/sec maximum leak rate
2. No organic materials in package
3. Capability of sealing package with controlled atmosphere
4. Must withstand severe military environment
5. Vertical interconnections required to interface drive circuitry with display
6. Compatibility of sealing process with thin film EL process
7. Conventional socket pin outs and end stackability required
8. Multiplexed digit operation capability.

6.2 Design and Fabrication

Figure 9 shows a cross section of the hermetic seal design. The design approach utilizes a frit seal to attach the sidewall frame to the substrate (580°C). The decoder driver electronics are then installed by conventional die attach and wire bond techniques as shown. Gold wire thermosonic bonding is used to bond the connections from the IC chips to the thick film conductor patterns previously applied. The vertical interconnect bars are then (AuSn) brazed in position (280°C). This assembly is then brazed to the EL display substrate, simultaneously brazing the vertical interconnect pads (280°C). Temperature gradients imposed during the second braze do not allow the connects at the lower ceramic substrate to reflow.

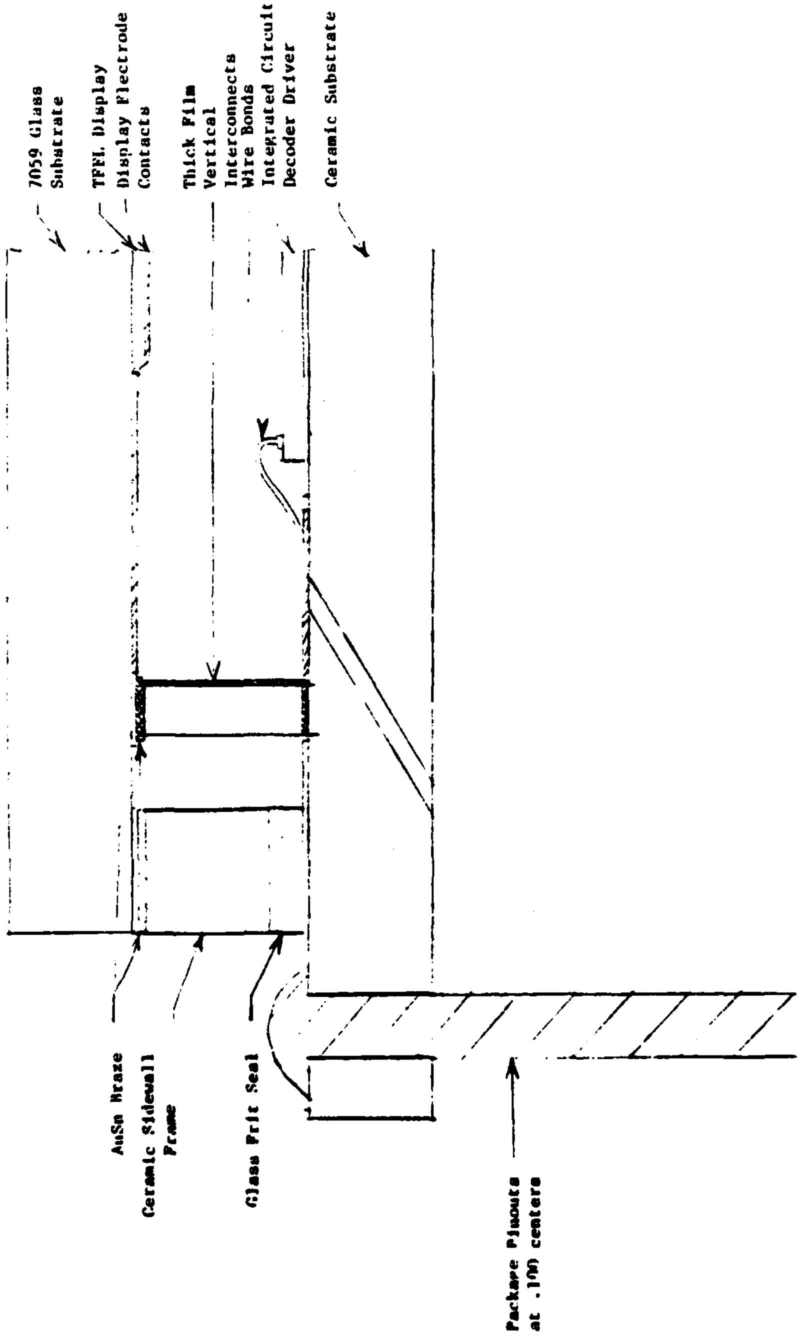


Fig. 9 Hermetic Seal Design

Finally, a controlled atmosphere is introduced in the package through a porthole in the ceramic substrate. The porthole is sealed by brazing over with a gold plated Kovar platelet.

The component parts of the package can be seen in Fig. 10. The substrate and interconnect bars have thick film conductors (PtAu) applied and the substrate also has a frit material applied for sealing to the sidewall frame. Figure 11 shows the frit sealed subassembly. The top surface of the sidewall frame also has a (PtAu) thick film conductor for use in the final (AuSn) braze seal. All braze seals can be accomplished in a controlled atmosphere sealing furnace so that fluxes are not required. Figure 12 shows a sealed package configuration containing the EL display.

The first sealed devices do not yet contain the integrated circuits as the IC's have not yet been received from the vendor.

Many packages have been assembled with excellent hermeticity ($<10^{-10}$ std cc/sec), and reliabe vertical interconnections. Devices with active EL displays have also been fabricated.

The characteristics of these displays are presently being evaluated, particularly in the area of operating lifetimes in the hermetically sealed package. These results will be reported in the near future.

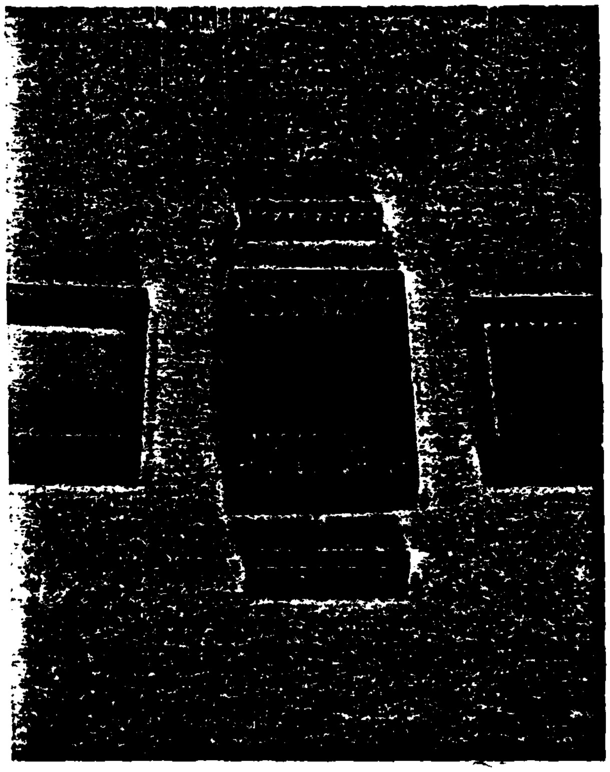


Fig. 10 Package Component Parts

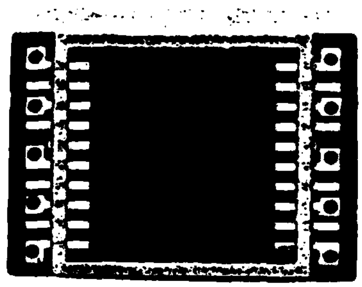


Fig. 11 Frit Sealed Subassembly

Fig. 12 Sealed Package Configuration

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